MICROSTAR LABORATORIES™

2265 116th Avenue N.E., Bellevue, WA 98004
Sales & Customer Support: (425) 453-2345
Finance & Administration: (425) 453-9489
Fax: (425) 453-3199
World Wide Web: http://www.mstarlabs.com/

Technical Product Information for the DAP 820™

The DAP 820 model

- has an onboard Intel 80C186XL 20 MHz processor
- works with the 16-bit ISA bus for x86/Pentium industry-standard PC platforms
- transfers data at high rates: up to 312k samples per second from a DAP 820 to the PC
- allows fast real-time processing
- offers low latency — 1 ms per task — for fast response
- samples analog or digital inputs at rates up to 312k samples per second
- updates two analog outputs at rates up to 312k samples per second each
- updates digital outputs at rates up to 312k samples per second

This technical note describes the DAP 820 in terms of software speed and functionality, special hardware characteristics, and similarities with other Data Acquisition Processor™ boards.

The DAP 820 is the lowest-priced Data Acquisition Processor board available from Microstar Laboratories™ and is appropriate for intelligent data acquisition and control applications where cost is more important than having spare capacity. With the DAP 820, Microstar Laboratories provides intelligent data acquisition and processing at the cost of a non-intelligent board. The DAP 820 provides all the standard DAPL™ commands available on other boards, performing them at rates appropriate for lower speed applications.

The onboard multitasking operating system, DAPL, provides a complete software environment for real-time data acquisition. DAPL is common to all Data Acquisition Processors and ensures that board-level hardware differences are transparent. To aid application development, DAPL comes complete with many system diagnostics, in addition to automatic memory and system checks that are done at initialization. Tasks that perform averaging, triggering, FFTs, filtering, arithmetic operations, and many other functions are pre-coded in DAPL. These tasks, or DAPL commands, are chained together to form a complete data acquisition application. Custom commands also can be written using the Developer's Toolkit for DAPL™ if multiple commands need to be combined or if a specific application cannot be implemented with standard DAPL commands.

The DAP 820 works with the 16-bit ISA bus for x86/Pentium industry-standard PC platforms. 1kB bidirectional first-in-first-out (BiFIFO) buffers allow fast data transfer to the host PC. For example, the DAP 820/103 can transfer information to the PC at rates as high as 312k samples per second.

The DAP 820 solves application problems at a low-cost. It has all the features needed for an entry-level data acquisition or control application with light real-time processing and expansion needs and provides all of the benefits of onboard intelligence. The DAP 820 makes an excellent choice for applications needing moderate real-time triggering, averaging, control, interpolation, or many other functions, but not high-speed FFTs or other computationally intensive operations. Table 1 gives information about the execution speed of DAPL commands on the DAP 820. For higher power applications, any of the DAP 3000a™, DAP 3200a™, DAP 3216a™, or DAP 3400a™ series may be appropriate. Contact Microstar Laboratories for more information on these products.

Table 1: DAPL command execution speed for the DAP 820 series

DAPL Command	Description of Use in Benchmark	Time of Execution[1] on DAP 820/103
`AVERAGE`	Averages groups of 16 data points[2]	70.4 µs
`FFT`	FFT of blocksize of 512 points	119 ms
`RFILTER`	Filters input data with 20 tap filter	157.6 µs
`LIMIT`	Generates level-based triggers on 1% of data	4.8 µs
`WAIT`	Processes data based upon triggers at a retention rate of 5 out of 100 samples	2.4 µs
DAPL Expression: `P3 = P1 + P2`	Adds two word-length pipe values together	30.8 µs

In addition to its processing capabilities, the DAP 820 provides a complete arrangement of analog and digital input and output sections. The analog input section is expandable—up to 32 single-ended or 16 differential inputs. See Table 2 for more information.

Each DAP 820 has an onboard 80C186XL processor. Data words are sent or received by the DMA controller of the 80C186XL at a rate of up to 312k samples per second. This data flow is clocked at a sampling rate or output rate controlled in software, but the actual rate is accurately set by onboard crystal-controlled timers. The sample period is specified in steps as small as a fifth of a microsecond. The length of every input sample period is accurate to 50 parts per million.

In addition to onboard timing, the DAP 820 also has provisions for external input and output triggers and an external clock input for input and output.

[1] The speed given is an actual application speed for the DAPL task, including sampling, DAPL task-switching and activation, and simulated transfer time. Kernel speeds for the tasks are actually faster.

[2] The speed given is for the complete block operation, if applicable. For a per value speed, the time of execution must be divided by the block size.

To clarify the operation for the various hardware sections, Figure 1 displays the architecture of the internal processing in the DAP 820.

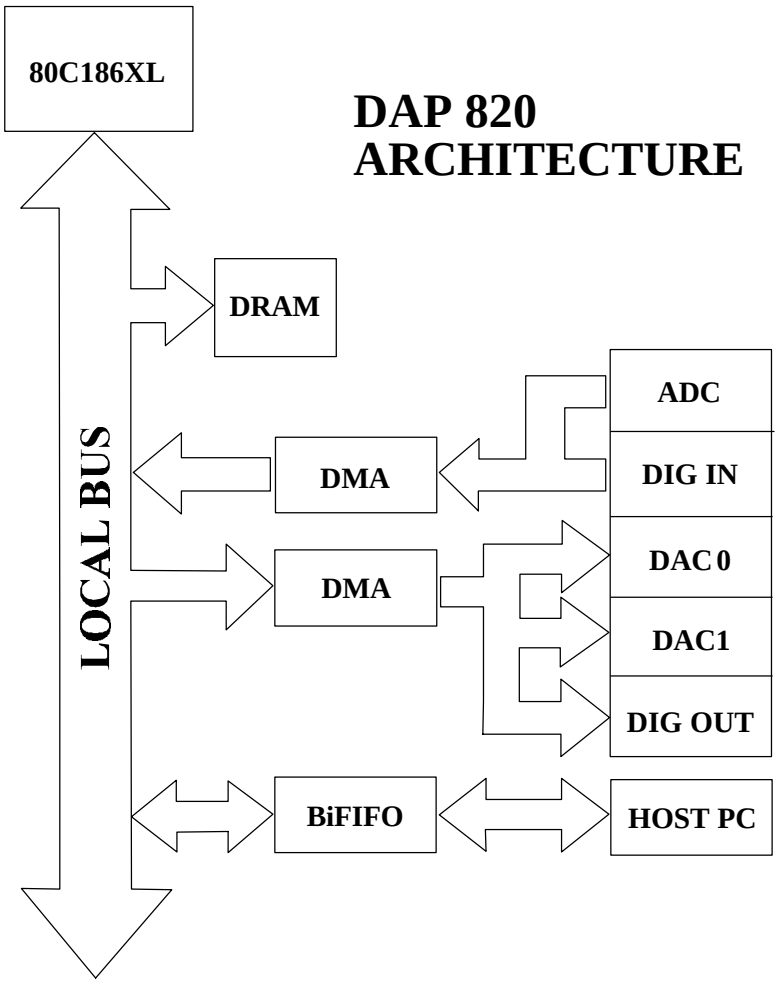

Figure 1: DAP 820 Data Acquisition Hardware

The 80C186XL processor, shown in Figure 1, performs the operations necessary for data acquisition and control. The CPU resides on the local DAP 820 bus and directs all data transfers. For instance, data from the analog and digital inputs are sent via DMA transfers to the onboard DRAM memory. From there data can be processed by the CPU, transferred to the PC, and/or directed via DMA to the output section.

Transfer of data and other communication to the PC is handled by a BiFIFO buffer. Information can be exchanged with the PC in both directions simultaneously and can be either DAPL programs, binary or text data, error messages, or DAPL system commands. This communication method is not only faster than DMA, but allows multiple Data Acquisition Processors to share one interrupt line. In this way, up to 14 Data Acquisition Processors can control and acquire data in one PC.

In addition to the processor and data transfer hardware, some important hardware specifications of the DAP 820 are given in Table 2 on the following pages.

Table 2: DAP 820/103 Typical Hardware Specifications

Specification	DAP 820/103
Dimensions	13.33" x 4.80"
Weight	9.3 oz
CPU Type	Intel 80C186XL
CPU Clock Speed	20 MHz
CPU DRAM	1 Mbyte
Data Acquisition Mode	DMA
Bus Support	16-bit AT ISA
PC Interface Hardware	1kByte BiFIFO buffer
PC Transfer Mode	I/O Interrupt
Maximum Transfer Rate	312k samples/sec
Power Requirements	+5V, 2.3 Amps
Operating Temperature	0-50 °C
Accuracy of Crystal Clocks	50 parts per million
Type of A⇒D Converter	Successive Approximation
Model of A⇒D Converter	Burr-Brown ADS7800
Max. Analog Sampling at Gain = 1 Gain = 10 Gain = 100 Gain = 500	 312k samples/sec 125k samples/sec 25k samples/sec 2k samples/sec
Number of Channels	8
Expandable To	32
Analog Input Voltage Ranges	0 to 5 V -5 to 5 V -10 to 10 V
Resolution If Range is -5 to 5 Volts	12 bits 2.4 mV
Accuracy If Range is -5 to 5 Volts	±1 LSB ±2.4 mV
Analog Input Bias Current	12 nA
Analog Input Impedance	>> 10 MΩ

Table 2: DAP 820/103 Typical Hardware Specifications cont.

Specification	DAP 820/103
Common Mode Rejection	90 dB
Max. Input Voltage	±25 V
Type of D⇒A Converter	Voltage Output
Model of D⇒A Converter	Burr-Brown DAC813
Maximum Update Rate	312k updates/sec
Number of Channels	2
Output Ranges	0 to 10 V -5 to 5 V -10 to 10 V
Resolution If Range is -5 to 5 volts	12 bits 2.4 mV
Accuracy If Range is -5 to 5 volts	±1 LSB, ±2.4 mV
Output Impedance	0.2 Ω
Current Source Maximum	±1 mA
Digital Input/Output Logic	FCT TTL
Max. Digital Update Rate	312k words/sec
Number of Input Bits Number of Output Bits	8 8
Digital Input Min. Logical High Max. Logical Low Max. Current Sink Max. Current Source	 2 V 0.8 V 20 µA 20 µA
Digital Output Min. Logical High Max. Logical Low Max. Current Sink Max. Current Source	 2.4 V 0.5 V 12 mA 15 mA
Hardware Clock Min. Pulse Width	25 ns
Hardware Trigger Min. Pulse Width	60 ns
Trigger Modes	GATED ONE-SHOT