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Technical Product Information for the DAP 2400a™

The DAP 2400a models

- each have an onboard Intel 80C186XL 16-MHz or 20-MHz processor
- each have a Motorola DSP56001 co-processor for FFTs and digital filtering
- are completely compatible with other a-Series boards
- work with the PC/AT/ISA bus for 286/386/486 PC and Pentium platforms
- transfer data at high rates—up to 312K samples per second
- allow fast real-time processing
- offer low latency—1 ms per task—for fast response
- sample analog or digital inputs at rates up to 312K samples per second
- update analog outputs at rates up to 312K samples per second each
- update digital outputs at rates up to 312K samples per second
- each have expandable analog and digital inputs/outputs

There are three DAP 2400a models: the DAP 2400a/4, the DAP 2400a/5, and the DAP 2400a/6. The differences between models include CPU speed, DSP speed, DSP memory size, and maximum sampling rate. This information is given in Table 3 at the end of this technote.

DSP speed and size of DSP memory are the key features for real-time digital signal processing applications. For instance, the DAP 2400a/6 is the only Data Acquisition Processor™ board able to perform FFTs with a block size of 8192 points. See Table 1 below for more information.

Table 1 : Maximum FFT Block Size for the DAP 2400a-Series

DAP 2400a Type	Maximum DSP FFT Size	Maximum FFT Block Size
DAP 2400a/4	512	2048
DAP 2400a/5	2048	2048
DAP 2400a/6	8192	8192

For the DAP 2400a/4, FFTs of block size larger than 512 are executed on the 80C186XL processor. This greatly reduces the speed of execution for these large FFT blocks in comparison to the other DAP 2400a-Series models. Smaller DSP computations, such as a 512 point FFT, are executed upon the Motorola DSP56001 for maximum performance.

The DAP 2400a provides high performance digital signal processing, yet the DAP 2400a is still completely compatible with a-Series boards and may be exchanged with them in any configuration.

The onboard multi-tasking operating system, DAPL™, is also common to all a-Series boards and ensures that hardware-level differences are transparent. DAPL is a complete software environment for real-time data acquisition. To aid application development, DAPL comes complete with many system diagnostics, in addition to automatic memory and system checks that are done at initialization. Tasks that perform averaging, triggering, fast fourier transforms, filtering, arithmetic operations, or many other functions are pre-coded in DAPL. These tasks, or DAPL commands, are chained together

to form a complete data aquisition application. Custom commands can also be written with the Developer's Toolkit for DAPL™ if multiple DAPL commands need to be combined or if a very specific application cannot be achieved with standard commands. In the table below, some standard DAPL commands are tabulated with their speed of execution on the DAP 2400a.

Table 2: Comparison of DAPL command speeds within the DAP 2400a-Series

DAPL Command	Description	Time of Execution[1] on DAP 2400a/4	Time of Execution on DAP 2400a/5	Time of Execution on DAP 2400a/6
`AVERAGE`	Averages groups of 16 data points[2]	88 µs	88 µs	70.4 µs
`FFT`	FFT of blocksize of 512 points	8.7 ms	6.9 ms	5.3 ms
`LIMIT`	Generates level based triggers on 1% of data	5.5 µs	5.5 µs	4.8 µs
`RFILTER`	Filters input data with 20 tap filter	15 µs	11.75 µs	9.4 µs
`WAIT`	Processes data based upon triggers at a retention rate of 5 out of 100 samples	3.75 µs	3.75 µs	2.4 µs
DAPL Expression: `P3 = P1 + P2`	Adds two word-length pipe values together	40.0 µs	40.0 µs	30.8 µs

Another common element shared by the a-Series boards is the bus interface. Like all a-Series boards, the DAP 2400a works with the PC/AT/ISA bus for 286/386/486 and Pentium platforms. On a -Series boards, 1K bidirectional FIFO buffers allow fast data transfer to and from the host PC. The maximum transfer rates for the DAP 2400a are 312K samples per second to send data to the PC, and up to 519K samples per second to transfer information from the PC

The main difference between the DAP 2400a and the other a-Series Data Acquisition Processors is that each of the DAP 2400a models has an onboard DSP co-processor in addition to the CPU. The DAP 2400a is therefore an excellent choice for applications where there is a need for real-time digital signal processing, such as FFTs, digital filtering, transfer functions, or correlations of sampled data. Table 2, on the previous page, gives information about the execution speed of DSP-related DAPL commands on the DAP 2400a.

In addition to high performance processing, the DAP 2400a provides the standard arrangement of complete analog/digital input and output sections. These analog and digital sections are completely expandable—see Table 3 for complete specifications.

Data is sent or received by the DMA controller of the 80C186XL at a rate of up to 312K samples per second. This data is clocked at a sampling rate or output rate controlled in software, but the actual rate

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[1] The speed given is an actual application speed for the DAPL task, including sampling, DAPL task-switching and activation, and simulated transfer time. Kernel speeds are actually faster.

[2] The speed given is for the complete block operation, if applicable. For a per value speed, divide the time of execution by the block size.

is accurately set by onboard crystal-controlled timers. The sample period is specified in steps as small as a fifth of a microsecond. The length of every sample period is accurate to 50 parts per million.

In addition to onboard timing, the DAP 2400a also has provisions for an external triggering and and clocking for the input and output sections.

Note that the digital and analog output sections of the DAP 2400a cannot be updated synchronously at the same time.

Figure 1 displays the architecture of the processing hardware of the DAP 2400a. Figure 1 shows the two processors which perform the operations necessary for data acquisition and control. These two processors both reside upon the local Data Acquisition Processor bus, and transfer information between each other and the analog/digital input and output sections. For instance, data from the analog and digital inputs are sent via DMA transfers to the CPU DRAM. From there it can be processed by the CPU, re-sent to the DSP56001 for further processing, transferred to the PC, and/or directed to the output section.

Transfer of data and other communication to the PC is handled by a BiFIFO. Information can be exchanged with the PC in both directions simultaneously, and can be either DAPL programs, binary or text data, error messages, or DAPL system commands. This communication method is not only faster than DMA, but allows multiple Data Acquisition Processor boards to share one interrupt line. In this way, up to fourteen DAP 2400a boards can control and aquire data in one PC.

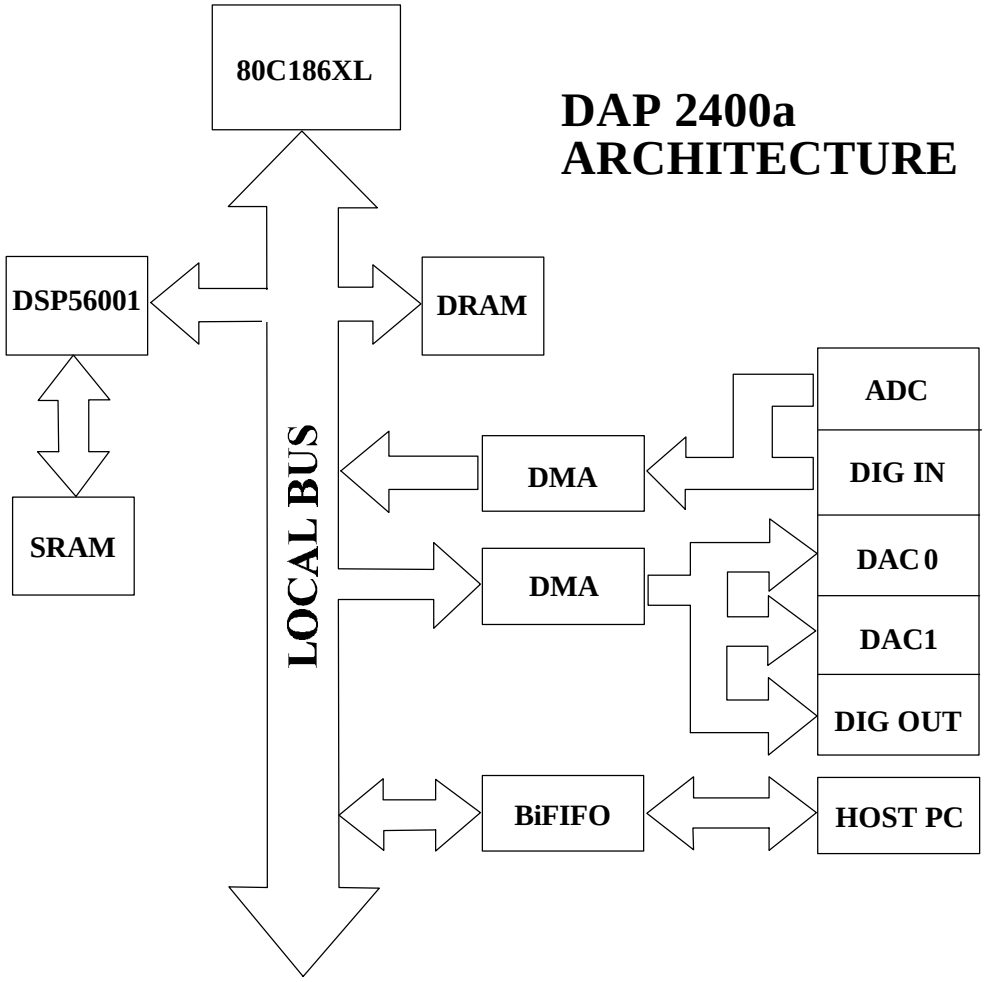

Figure 1: DAP 2400a Data Acquisition Hardware

In addition to the processors and data transfer hardware, some other important hardware specifications of the DAP 2400a are given on the next page.

Table 3: DAP 2400a Typical Hardware Specifications

Specification	DAP 2400a/4	DAP 2400a/5	DAP 2400a/6
Dimensions	13.33" x 4.8"	13.33" x 4.8"	13.33" x 4.8"
Weight	10.3 oz	10.3 oz	10.3 oz
CPU Type	Intel 80C186XL	Intel 80C186XL	Intel 80C186XL
CPU Clock Speed	16 MHz	16 MHz	20 MHz
CPU DRAM	1 Mbyte	1 Mbyte	1 Mbyte
DSP Type	Motorola DSP56001	Motorola DSP56001	Motorola DSP56001
DSP Clock Speed	20 MHz	27 MHz	32 MHz
DSP SRAM	6 Kbytes	24 Kbytes	96 Kbytes
DSP⇔CPU transfer speed	1.8 MBytes/sec	3.6 MBytes/sec	5.0 MBytes/sec
Data Acquisition Mode	DMA	DMA	DMA
Bus Support	AT	AT	AT
PC Interface Hardware	Dual 512 byte FIFOs	Dual 512 byte FIFOs	Dual 512 byte FIFOs
PC Transfer Mode	I/O Interrupt	I/O Interrupt	I/O Interrupt
Maximum Transfer Rate	166K samples/sec	250K samples/sec	312K samples/sec
Power Requirements	+5V, 2.5 Amps	+5V, 2.5 Amps	+5V, 2.5 Amps
Operating Temperature	0-50 °C	0-50 °C	0-50 °C
Accuracy of Crystal Clocks	50 parts per million	50 parts per million	50 parts per million
Type of A⇒D Converter	Successive Approximation	Successive Approximation	Successive Approximation
Model of A⇒D Converter	Burr-Brown ADS7800	Burr-Brown ADS7800	Burr-Brown ADS7800
Max. Analog Sampling at Gain = 1 Gain = 10 Gain = 100 Gain = 500	 166 K samples/sec 125 K samples/sec 25 K samples/sec 2 K samples/sec	 250 K samples/sec 125 K samples/sec 25 K samples/sec 2 K samples/sec	 312 K samples/sec 125 K samples/sec 25 K samples/sec 2 K samples/sec
Number of Analog Channels	16	16	16
Expandable To	512	512	512
Input Voltage Ranges	0 to 5 V -5 to 5 V -10 to 10 V	0 to 5 V -5 to 5 V -10 to 10 V	0 to 5 V -5 to 5 V -10 to 10 V
Resolution If Range is -5 to 5 Volts	12 bits 2.4 mV	12 bits 2.4 mV	12 bits 2.4 mV
Accuracy If Range is -5 to 5 Volts	±1 LSB ±2.4 mV	±1 LSB ±2.4 mV	±1 LSB ±2.4 mV
Bias current	12 nA	12 nA	12 nA
Analog Input Impedance	>> 10 MΩ	>> 10 MΩ	>> 10 MΩ
Common Mode Rejection	90 dB	90 dB	90 dB
Max. Input Voltage (Fault-protected)	±25 V	±25 V	±25 V

Table 3: DAP 2400a Typical Hardware Specifications, continued

Specification	DAP 2400a/4	DAP 2400a/5	DAP 2400a/6
Type of D⇒A Converter	Voltage Output	Voltage Output	Voltage Output
Model of D⇒A Converter	Burr-Brown DAC813	Burr-Brown DAC813	Burr-Brown DAC813
Maximum Update Rate	166K updates/sec[3]	250K updates/sec	312K updates/sec
Number of Channels	2	2	2
Expandable To	66	66	66
Output Ranges	0 to 10 V -5 to 5 V -10 to 10 V	0 to 10 V -5 to 5 V -10 to 10 V	0 to 10 V -5 to 5 V -10 to 10 V
Resolution If Range is -5 to 5 volts	12 bits 2.4 mV	12 bits 2.4 mV	12 bits 2.4 mV
Accuracy If Range is -5 to 5 volts	±1 LSB, ±2.4 mV	±1 LSB, ±2.4 mV	±1 LSB, ±2.4 mV
Output Impedance	0.05 Ω	0.05 Ω	0.05 Ω
Current Source Maximum	±1 mA	±1 mA	±1 mA
Digital I/O Logic	FCT TTL	FCT TTL	FCT TTL
Max. Digital Update Rate	166K words/sec	250K words/sec	312K words/sec
Number of Input Bits Number of Output Bits	16 16	16 16	16 16
Expandable To	128 bits of input and 1024 bits of output	128 bits of input and 1024 bits of output	128 bits of input and 1024 bits of output
Digital Input Min. Logical High Max. Logical Low Max. Current Sink Max. Current Source	 2 V 0.8 V 20 µA 20 µA	 2 V 0.8 V 20 µA 20 µA	 2 V 0.8 V 20 µA 20 µA
Digital Output Min. Logical High Max. Logical Low Max. Current Sink Max. Current Source	 2.6 V 0.5 V 24 mA 2.6 mA	 2.6 V 0.5 V 24 mA 2.6 mA	 2.6 V 0.5 V 24 mA 2.6 mA
Hardware Clock Min. Pulse Width	25 ns	25 ns	25 ns
Hardware Trigger Min. Pulse Width	60 ns	60 ns	60 ns
Trigger Modes	GATED ONE-SHOT	GATED ONE-SHOT	GATED ONE-SHOT

[3] The DAP 2400a can update each of its two standard analog outputs independently at the maximum update rate specified. When analog output expansion is used, the update rate for expanded channels is determined by :

Expanded Analog Output Rate = Max Digital Update Rate / (4 * Number of Channels)