MICROSTAR LABORATORIES™

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Technical Note TN-168 **Version 1.3**

DAP 1216a™ and DAP 2416a™ Typical Hardware Specifications

Specification	DAP 1216a/6	DAP 2416a/6
Dimensions	13.33" x 4.8"	13.33" x 4.8"
Weight	9.9 oz	10.3 oz
CPU Type	Intel 80C186XL	Intel 80C186XL
CPU Clock Speed	20 MHz	20 MHz
CPU DRAM	1 Mbyte	1 Mbyte
DSP Type	na	Motorola DSP56001
DSP Clock Speed	na	32 MHz
DSP SRAM	na	96 Kbytes
DSP⇔CPU transfer speed	na	5.0 MBytes/sec
Data Acquisition Mode	DMA	DMA
Bus Support	AT, EISA compatible	AT, EISA compatible
PC Interface Hardware	Dual 512 byte FIFOs	Dual 512 byte FIFOs
PC Transfer Mode	I/O Interrupt	I/O Interrupt
Maximum Transfer Rate	312K samples/sec	312K samples/sec
Power Requirements	+5V, 3.0 Amps	+5V, 3.0 Amps
Operating Temperature	0-50 °C	0-50 °C
Accuracy of Crystal Clocks	50 parts per million	50 parts per million
Type of A⇒D converter	Analog Devices AD976	Analog Devices AD976
Max. Analog Sampling at Gain = 1 Gain = 10 Gain = 100 Gain = 500	 100 K samples/sec 100 K samples/sec 17 K samples/sec 2 K samples/sec	 100 K samples/sec 100 K samples/sec 17 K samples/sec 2 K samples/sec
Number of Channels	16	16
Expandable To	64	64
Input Voltage Ranges	-5 to 5 V -10 to 10 V	-5 to 5 V -10 to 10 V
Resolution If Range is -5 to 5 Volts	16 bits 150 μV	16 bits 150 μV
Input Integral Nonlinearity	±2 LSB	±2 LSB
Input Differential Nonlinearity	±2 LSB	±2 LSB
Input Noise	±3.5 LSB*	±3.5 LSB*
Input Impedance	>> 10 MΩ	>> 10 MΩ
Common Mode Rejection	98 dB	98 dB
Max. Input Voltage	±25 V	±25 V

* Accuracy may be increased by minimizing the input noise contribution to error. This is done by filtering data on the Data Acquisition Processor.

DAP 1216a and DAP 2416a Typical Hardware Specifications, *continued*

Specification	DAP 1216a/6	DAP 2416a/6
Type of D⇒A Converter	Analog Devices AD669	Analog Devices AD669
Maximum Update Rate	125K updates/sec**	125K updates/sec**
Number of Channels	2	2
Expandable To	66	66
Output Ranges	-5 to 5 V -10 to 10 V	-5 to 5 V -10 to 10 V
Resolution If Range is -5 to 5 volts	16 bits 150 µV	16 bits 150 µV
Ouput Integral Nonlinearity	±2 LSB	±2 LSB
Output Differential Nonlinearity	±2 LSB	±2 LSB
Output Temperature Drift	±1.5 LSB per °C	±1.5 LSB per °C
Current Source Maximum	± 1 mA	± 1 mA
Digital Logic	FCT TTL	FCT TTL
Max. Digital Updates/sec.	166K words/sec	312K words/sec
Number of Input Bits Number of Output Bits	16 16	16 16
Expandable To	128 bits of input and 1024 bits of output	128 bits of input and 1024 bits of output
Digital Input		
Min. Logical High Max. Logical Low Max. Current Sink Max. Current Source	2 V 0.8 V 20 µA 20 µA	2 V 0.8 V 20 µA 20 µA
Digital Output		
Min. Logical High Max. Logical Low Max. Current Sink Max. Current Source	2.4 V 0.5 V 12 mA 15 mA	2.4 V 0.5 V 12 mA 15 mA
Hardware Clock Min. Pulse Width	25 ns	25 ns
Hardware Trigger Min. Pulse Width	60 ns	60 ns
Trigger Modes	GATED ONE-SHOT	GATED ONE-SHOT

** The DAP 1216a and DAP 2416a can update each of its two standard analog outputs independently at the maximum update rate specified. This maximum update rate is set from the measured full scale settling time of 8 us (0.5 LSB accuracy). For small changes between updates, a higher update rate can be maintained. When analog output expansion is used, the update rate for expanded channels is determined by :

Expanded Analog Output Rate = Max Digital Update Rate / (4 * Number of Channels)