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Technical Product Information for the DAP 800™

The DAP 800 models

- each have an on-board Intel 80C188XL 10-MHz or 16-MHz processor.
- work with the XT/PC/AT/ISA bus for 8086/286/386/486 and Pentium PC platforms.
- transfer data at high rates: up to 105K samples per second from a DAP 800 to the PC.
- allow fast real-time processing.
- offer low latency — 1 ms per task — for fast response.
- sample analog or digital inputs at rates up to 105K samples per second.
- update two analog outputs at rates up to 105K samples per second each.
- update digital outputs at rates up to 105K samples per second.

This technical note describes all of the DAP 800 models in terms of software speed and functionality, special hardware characteristics, and similarities with other Data Acquisition Processor™ boards.

There are three DAP 800 models: the DAP 801/101, the DAP 800/102, and the DAP 800/103. Their hardware differs mostly in three areas: speed of the on-board CPU, DRAM size, and sampling rate. These specifications are compared in Table 2 — "DAP 800 Typical Hardware Specifications."

The DAP 801/101 has the added feature of a serial connector which allows it to communicate with the PC in stand-alone mode. Ask for Microstar Laboratories Technical Note TN-158 for more information on configuring the DAP 801/101 in stand-alone mode.

The DAP 800 is the lowest-priced Data Acquisition Processor board available from Microstar Laboratories, and is appropriate for intelligent data acquisition and control applications where cost is important. With the DAP 800, Microstar Laboratories provides intelligent data acquisition and processing at the cost of a non-intelligent board. The DAP 800 provides all the standard DAPL™ commands available on other boards, performing them at rates appropriate for lower speed applications.

The on-board multi-tasking operating system, DAPL, is a complete software environment for real-time data acquisition. DAPL is common to all Data Acquisition Processors and ensures that board-level hardware differences are transparent. To aid application development, DAPL comes complete with many system diagnostics, in addition to automatic memory and system checks that are done at initialization. Tasks that perform averaging, triggering, FFTs, filtering, arithmetic operations, and many other functions are pre-coded in DAPL. These tasks, or DAPL commands, are chained together to form a complete data aquisition application. Custom commands also can be written with the Advanced Development Toolkit if multiple commands need to be combined or if a specific application cannot be implemented with standard DAPL commands.

Another common element shared by the DAP 800 series is the bus interface. The DAP 800 models work with both XT and AT ISA busses for 286/386/486 and Pentium PC platforms. 256-byte first-in-

first-out (FIFO) buffers allow fast data transfer to the host PC. For example, the DAP 800/102 and DAP 800/103 can transfer information to the PC at rates as high as 105K samples per second.

The main feature of the DAP 800 is its ability to solve applications at a low-cost. The DAP 800 is an excellent choice for applications where there is a need for moderate real-time triggering, averaging, control, interpolation, or many other functions, but no need for high-speed FFTs or other computationally intensive operations. Table 1 gives information about the execution speed of DAPL commands on the DAP 800. For higher power applications, any of the DAP 1200e™, DAP 2400e™, DAP 1216e™, DAP 2416e™, or DAP 3200e™ series may be appropriate. Contact Microstar Laboratories for more information on these products.

Table 1: DAPL command execution speed for the DAP 800 series

DAPL Command	Description	Time of Execution[1] on DAP 801/101	Time of Execution on DAP 800/102 or DAP 800/103
`AVERAGE`	Averages groups of 16 data points[2]	345.6 µs	152 µs
`FFT`	FFT of blocksize of 512 points	463 ms	247 ms
`RFILTER`	Filters input data with 20 tap filter	580.4 µs	316 µs
`LIMIT`	Generates level based triggers on 1% of data	12.4 µs	7 µs
`WAIT`	Processes data based upon triggers at a retention rate of 5 out of 100 samples	14 µs	6 µs
DAPL Expression: `P3 = P1 + P2`	Adds two word-length pipe values together	174.4 µs	64 µs

In addition to its processing capabilities, the DAP 800 provides a complete arrangement of analog and digital input and output sections. The analog input section is expandable—up to 32 single-ended or 16 differential inputs. See Table 2 for more information.

Data is sent or received by the DMA controller of the 80C188XL at a rate of up to 105K samples per second. This data is clocked at a sampling rate or output rate controlled in software, but the actual rate is accurately set by on-board crystal-controlled timers. The sample period is specified in steps as small as a quarter of a microsecond. The length of every sample period is accurate to 50 parts per million.

In addition to on-board timing, the DAP 800 also has provisions for an external input trigger and an external clock input for input and output.

[1] The speed given is an actual application speed for the DAPL task, including sampling, DAPL task-switching and activation, and simulated transfer time. Kernel speeds for the tasks are actually faster.

[2] The speed given is for the complete block operation, if applicable. For a per value speed, the time of execution must be divided by the block size.

To clarify the operation for the various hardware sections, Figure 1 displays the architecture of the internal processing in the DAP 800.

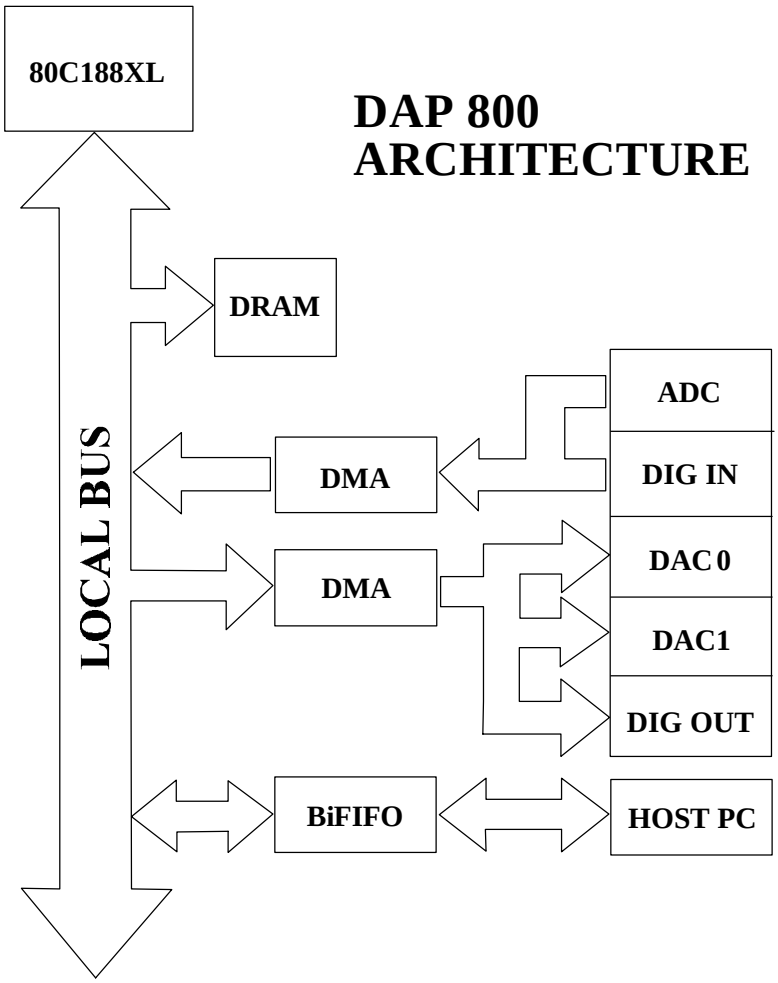

Figure 1: DAP 800 Data Acquisition Hardware

The 80C188XL processor, shown in Figure 1, performs the operations necessary for data acquisition and control. The CPU resides on the local DAP 800 bus and directs all data transfers. For instance, data from the analog and digital inputs are sent via DMA transfers to the on-board DRAM memory. From there it can be processed by the CPU, transferred to the PC, and/or directed via DMA to the output section.

Transfer of data and other communication to the PC is handled by a FIFO buffer. Information can be exchanged with the PC in both directions simultaneously and can be either DAPL programs, binary or text data, error messages, or DAPL system commands. This communication method is not only faster than DMA, but allows multiple Data Acquisition Processors to share one interrupt line. In this way, up to 14 Data Acquisition Processors can control and acquire data in one PC.

In addition to the processor and data transfer hardware, some important hardware specifications of the DAP 800 are given in Table 2 on the following pages.

Table 2: DAP 800 Typical Hardware Specifications

Specification	DAP 801/101	DAP 800/102	DAP 800/103
Dimensions	13.37" x 4.2"	13.37" x 4.2"	13.37" x 4.2"
Weight	9.1 oz	9.1 oz	9.1 oz
CPU Type	Intel 80C188XL	Intel 80C188XL	Intel 80C188XL
CPU Clock Speed	10 MHz	16 MHz	16 MHz
CPU DRAM	256 Kbytes	256 Kbytes	1 Mbyte
Data Acquisition Mode	DMA	DMA	DMA
Bus Support[3]	XT, AT	XT, AT	XT, AT
PC Interface Hardware	256 byte FIFO	256 byte FIFO	256 byte FIFO
PC Transfer Mode	I/O Interrupt	I/O Interrupt	I/O Interrupt
Maximum Transfer Rate[4]	75K samples/sec	105K samples/sec	105K samples/sec
Power Requirements	+5V, 2.0 Amps	+5V, 2.0 Amps	+5V, 2.0 Amps
Operating Temperature	0-50 °C	0-50 °C	0-50 °C
Accuracy of Crystal Clocks	50 parts per million	50 parts per million	50 parts per million
Type of A⇒D Converter	Successive Approximation	Successive Approximation	Successive Approximation
Model of A⇒D Converter	Maxim MAX163	Maxim MAX163	Maxim MAX163
Max. Analog Sampling at Gain = 1 Gain = 10 Gain = 100 Gain = 500	 75 K samples/sec 75 K samples/sec 25 K samples/sec 2 K samples/sec	 105 K samples/sec 100 K samples/sec 25 K samples/sec 2 K samples/sec	 105 K samples/sec 100 K samples/sec 25 K samples/sec 2 K samples/sec
Number of Channels	8	8	8
Expandable To	32	32	32
Analog Input Voltage Ranges	-2.5 to +2.5 V 0 to 5 V -5 to 5 V -10 to 10 V	-2.5 to +2.5 V 0 to 5 V -5 to 5 V -10 to 10 V	-2.5 to +2.5 V 0 to 5 V -5 to 5 V -10 to 10 V
Resolution If Range is -5 to 5 Volts	12 bits 2.4 mV	12 bits 2.4 mV	12 bits 2.4 mV
Accuracy If Range is -5 to 5 Volts	±1 LSB ±2.4 mV	±1 LSB ±2.4 mV	±1 LSB ±2.4 mV
Analog Input Bias Current	12 nA	12 nA	12 nA
Analog Input Impedance	>> 10 MΩ	>> 10 MΩ	>> 10 MΩ

[3] The DAP 801/101 also can communicate in stand-alone mode via an RS-232 connection.

[4] When used in stand-alone mode, the DAP 801/101 can transfer data at a maximum rate of 100 samples per second.

Table 2: DAP 800 Typical Hardware Specifications cont.

Specification	DAP 800/1 or DAP 801/1	DAP 800/2	DAP 800/3
Common Mode Rejection	90 dB	90 dB	90 dB
Max. Input Voltage	±25 V	±25 V	±25 V
Type of D⇒A Converter	Voltage Output	Voltage Output	Voltage Output
Model of D⇒A Converter	Burr-Brown DAC811	Burr-Brown DAC811	Burr-Brown DAC811
Maximum Update Rate	75K updates/sec	105K updates/sec	105K updates/sec
Number of Channels	2	2	2
Output Ranges	0 to 10 V -5 to 5 V -10 to 10 V	0 to 10 V -5 to 5 V -10 to 10 V	0 to 10 V -5 to 5 V -10 to 10 V
Resolution If Range is -5 to 5 volts	12 bits 2.4 mV	12 bits 2.4 mV	12 bits 2.4 mV
Accuracy If Range is -5 to 5 volts	±1 LSB, ±2.4 mV	±1 LSB, ±2.4 mV	±1 LSB, ±2.4 mV
Output Impedance	0.2 Ω	0.2 Ω	0.2 Ω
Current Source Maximum	±1 mA	±1 mA	±1 mA
Digital Input/Output Logic	ALS TTL	ALS TTL	ALS TTL
Max. Digital Update Rate	75K words/sec	105K words/sec	105K words/sec
Number of Input Bits Number of Output Bits	8 8	8 8	8 8
Digital Input Min. Logical High Max. Logical Low Max. Current Sink Max. Current Source	 2 V 0.8 V 20 µA 20 µA	 2 V 0.8 V 20 µA 20 µA	 2 V 0.8 V 20 µA 20 µA
Digital Output Min. Logical High Max. Logical Low Max. Current Sink Max. Current Source	 2.6 V 0.5 V 24 mA 2.6 mA	 2.6 V 0.5 V 24 mA 2.6 mA	 2.6 V 0.5 V 24 mA 2.6 mA
Hardware Clock Min. Pulse Width	25 ns	25 ns	25 ns
Hardware Trigger Min. Pulse Width	60 ns	60 ns	60 ns
Trigger Modes	GATED ONE-SHOT	GATED ONE-SHOT	GATED ONE-SHOT